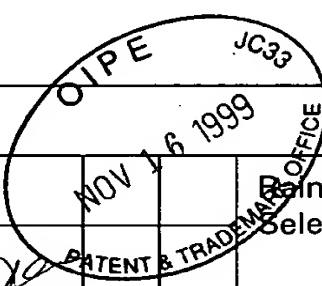


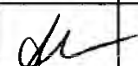
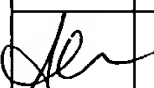


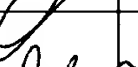
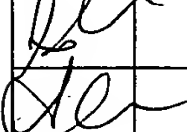
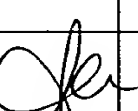
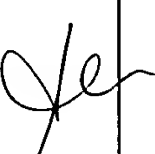
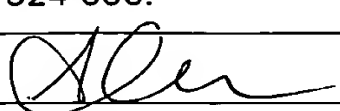


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11/11/99 HP10981866-1

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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | Docket: HP10981866-1 | | App: 09/378,596 | |
| | | Applicant: Gupta et al. | | | |
| | | Filed: August 20, 1999 | | RECEIVED Art Unit: 20 1999 Group 2700 | |
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| EXAMINER: | |  | | DATE 9/15/02 | |
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FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
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STATEMENT

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ATTY. DOCKET NO.

hp10981866-1

SERIAL NO.

09/378,596

APPLICANT

Gupta et al.

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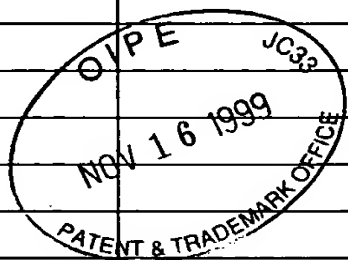
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REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS |
|---------------------|--------------------|------|------|-------|--------------|
| | 1A | | | | |
| | 1B | | | | |
| | 1C | | | | |
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FOREIGN PATENT DOCUMENTS

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| | | | | | | YES | NO |
| | 1L | | | | | | |
| | 1M | | | | | | |
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PATENT APPLICATION

Sheet 1 of 1

FORM PTO-159

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10981866-1

APPLICATION NO.

09/378,596

CONFIRMATION NO.

APPLICANT

Gupta, Shail Aditya, et al

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8/20/1999

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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

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